WHAT IS CLAIMED IS:

1. A testing device for testing an electronic device, comprising:

a deterministic jitter application unit operable to apply deterministic jitter to a given input signal without causing an amplitude modulation component and supply said input signal to said electronic device;

a jitter amount controller operable to control magnitude of said deterministic jitter generated by said deterministic jitter application unit; and

a determination unit operable to determine whether or not said electronic device is defective based on an output signal output from said electronic device in accordance with said input signal.

2. A testing device as claimed in claim 1, wherein said deterministic jitter application unit includes a primary filter operable to transmit said input signal and generate said deterministic jitter.

3. A testing device as claimed in claim 1, wherein said deterministic jitter application unit includes a cable operable to transmit said input signal and generate said deterministic jitter.

4. A testing device as claimed in claim 1, wherein said jitter amount controller determines said magnitude of said deterministic jitter based on a threshold value of a peak-to-peak value of alignment jitter between said input signal and a recovered clock signal recovered by said electronic device from

said input signal.

5. A testing device as claimed in claim 1, further comprising a sinusoidal jitter application unit operable to apply sinusoidal jitter to said input signal, wherein

said jitter amount controller further controls magnitude of said sinusoidal jitter generated by said sinusoidal jitter application unit.

6. A testing device as claimed in claim 5, wherein said jitter amount controller determines said magnitude of said sinusoidal jitter based on a threshold value of a peak-to-peak value of alignment jitter between said input signal and a recovered clock signal recovered by said electronic device from said input signal, and a jitter transfer function in a nondefective electronic device.

7. A testing device as claimed in claim 6, wherein said jitter amount controller determines said magnitude of said sinusoidal jitter based on a sinusoidal jitter threshold value obtained by multiplying said threshold value of said peak-to-peak value of said alignment jitter by a sinusoidal jitter ratio that is predetermined, and said jitter transfer function, and

determines said magnitude of said deterministic jitter based on a deterministic jitter threshold value obtained by subtracting said sinusoidal jitter threshold value from said threshold value of said peak-to-peak value of said alignment jitter, and said jitter transfer function.

8. A testing device as claimed in claim 6, wherein said jitter amount controller includes a jitter transfer function estimation

unit operable to obtain said jitter transfer function based on a timing jitter series of said input signal and a timing jitter series of said recovered clock signal recovered by said electronic device from said input signal.

9. A testing device as claimed in claim 6, wherein said sinusoidal jitter application unit applies said sinusoidal jitter having a plurality of frequency components to said input signal, and

said jitter amount controller determines magnitude of each of said frequency components of said sinusoidal jitter based on said threshold value of said peak-to-peak value of said alignment jitter and said jitter transfer function.

10. A testing device as claimed in claim 9, wherein said jitter amount controller determines said magnitude of each of said plurality of frequency components of said sinusoidal jitter based on a frequency-component threshold value obtained by multiplying said threshold value of said peak-to-peak value of said alignment jitter by a frequency-component ratio that is predetermined for that frequency component, and said jitter transfer function, and

determines said magnitude of said deterministic jitter based on a deterministic jitter threshold value obtained by subtracting a sum of said frequency-components threshold values corresponding to said plurality of frequency components, from said threshold value of said peak-to-peak value of said alignment jitter.

11. A testing device as claimed in claim 1, wherein said electronic device receives said input signal and a reference

clock signal as its input and samples said input signal based on said reference clock signal, wherein said testing device further comprises a phase shifter operable to shift a phase of said reference clock signal.

12. A testing device for testing an electronic device, comprising:

a sinusoidal jitter application unit operable to apply sinusoidal jitter to a given input signal and supply said input signal with said sinusoidal jitter to said electronic device;

a jitter amount controller operable to control magnitude of said sinusoidal jitter applied by said sinusoidal jitter application unit; and

a determination unit operable to determine whether or not said electronic device is defective based on an output signal output from said electronic device in accordance with said input signal, wherein

said jitter amount controller determines said magnitude of said sinusoidal jitter based on a threshold value of a peak-to-peak value of alignment jitter between said input signal and a recovered clock signal recovered by said electronic device from said input signal, and a jitter transfer junction in said electronic device that is nondefective.

13. A testing method for testing an electronic device, comprising:

applying deterministic jitter to a given input signal without causing an amplitude modulation component and supplying said input signal with said deterministic jitter to said electronic device;

controlling magnitude of said deterministic jitter applied

in the application of said deterministic jitter; and

determining whether or not said electronic device is defective based on an output signal output from said electronic device in accordance with said input signal.

14. A testing method as claimed in claim 13, wherein said deterministic jitter is generated by using a primary filter that transmit said input signal in said application of said deterministic jitter.

15. A testing method as claimed in claim 13, wherein said deterministic jitter is generated by using a cable that transmits said input signal in said application of said deterministic jitter.

16. A testing method as claimed in claim 13, further comprising applying sinusoidal jitter to said input signal.

17. A testing method as claimed in claim 16, wherein said sinusoidal jitter having a plurality of frequency components is applied to said input signal in said application of said sinusoidal jitter.

18. A testing method for testing an electronic device, comprising:

applying sinusoidal jitter to a given input signal and supplying said input signal with said sinusoidal jitter to said electronic device;

controlling magnitude of said sinusoidal jitter applied in said application of said sinusoidal jitter; and

determining whether or not said electronic device is

defective based on an output signal output from said electronic device in accordance with said input signal, wherein

said controlling of said magnitude of said sinusoidal jitter determines said magnitude of said sinusoidal jitter based on a threshold value of a peak-to-peak value of alignment jitter between said input signal and a recovered clock signal recovered by said electronic device from said input signal, and a jitter transfer function of said electronic device that is nondefective.